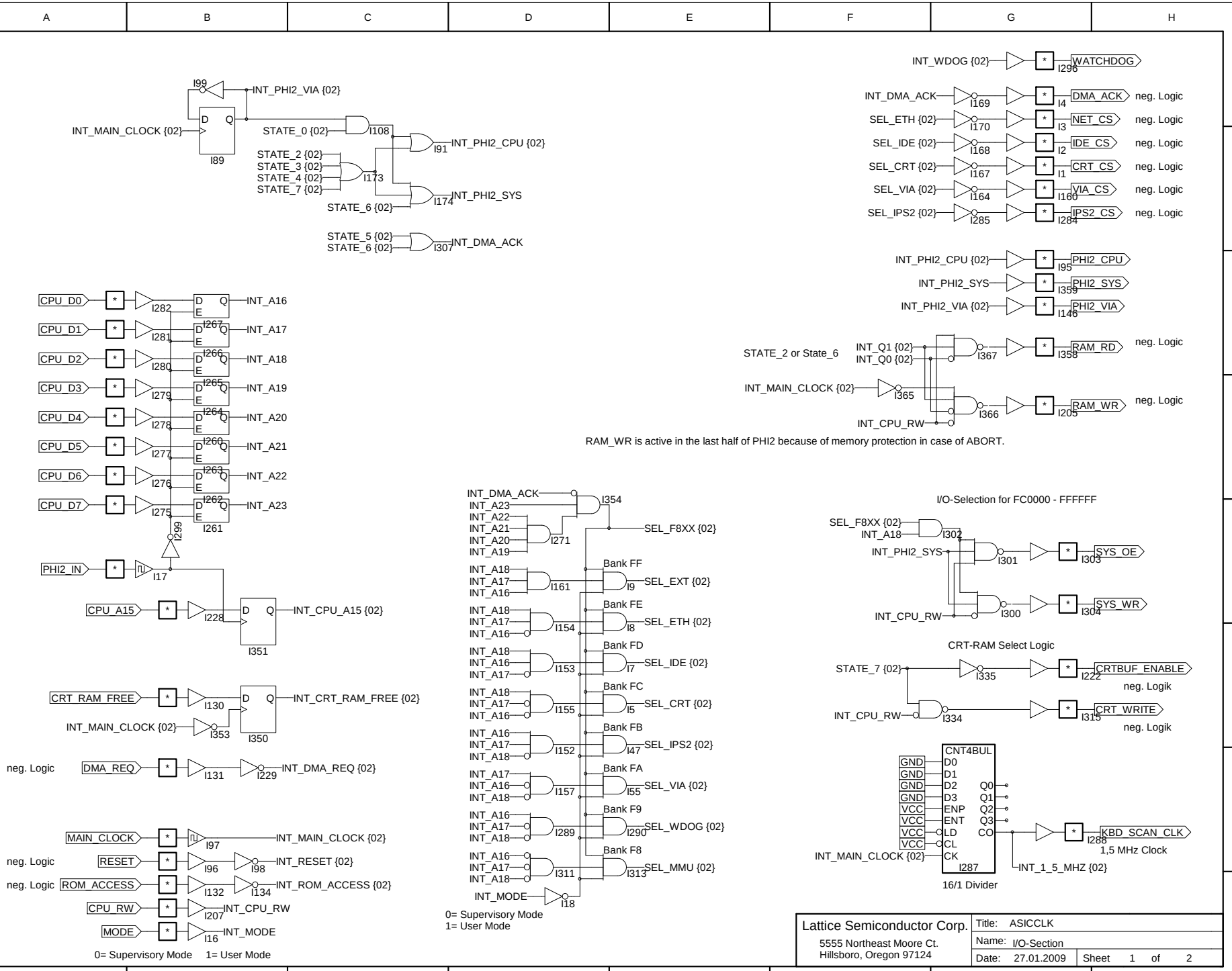
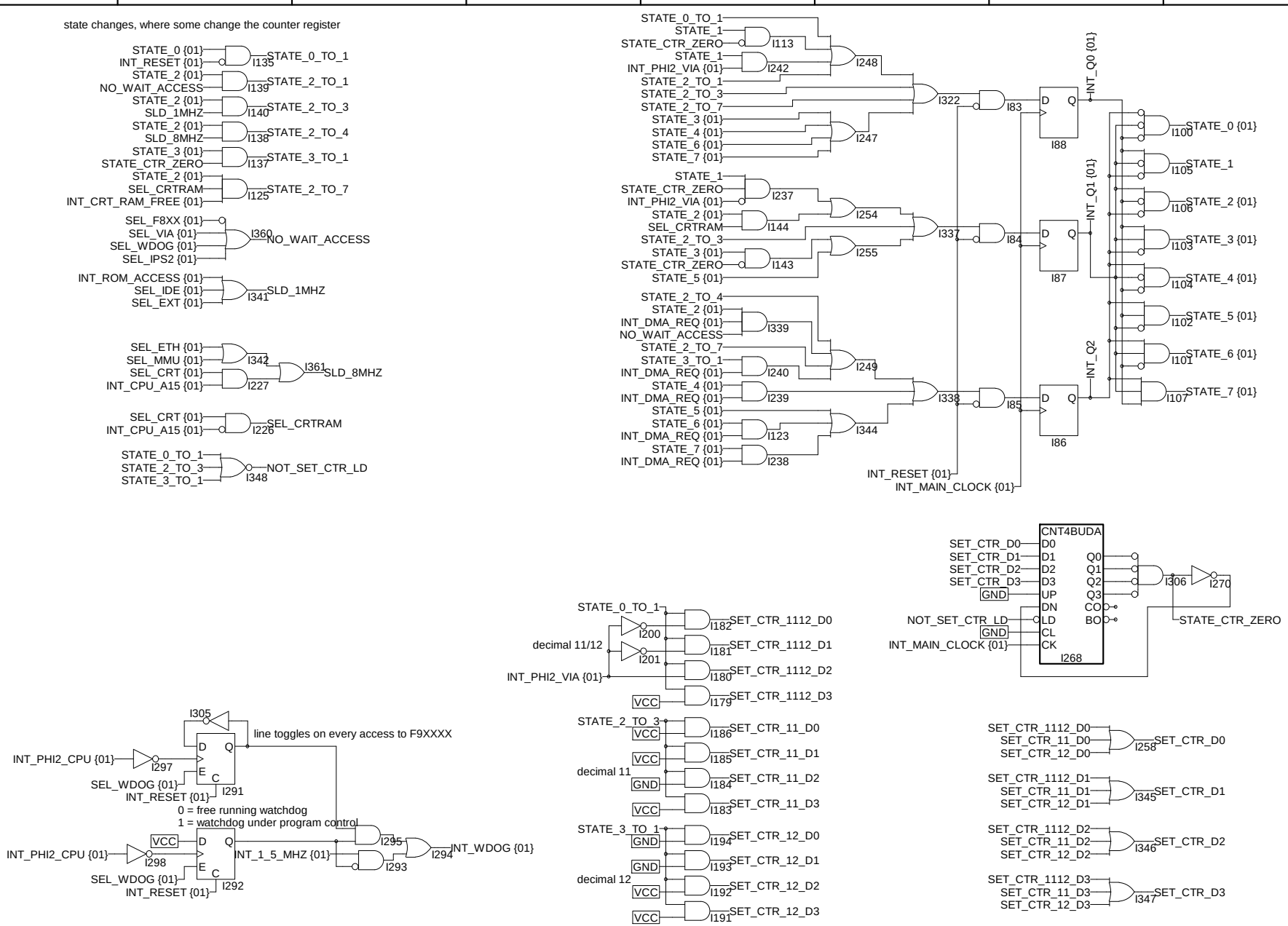

INT_PHI2_VIA {02}
I99
INT_MAIN_CLOCK {02}
D Q
I89
STATE_0 {02}
I108
STATE_2 {02}
STATE_3 {02}
STATE_4 {02}
STATE_7 {02}
I173
I91
INT_PHI2_CPU {02}
STATE_6 {02}
I174
INT_PHI2_SYS
STATE_5 {02}
STATE_6 {02}
I307
INT_DMA_ACK
INT_WDOG {02}
I296
WATCHDOG
INT_DMA_ACK
I169
I4
DMA_ACK
neg. Logic
SEL_ETH {02}
I170
I3
NET_CS
neg. Logic
SEL_IDE {02}
I168
I2
IDE_CS
neg. Logic
SEL_CRT {02}
I167
I1
CRT_CS
neg. Logic
SEL_VIA {02}
I164
I160
VIA_CS
neg. Logic
SEL_IPS2 {02}
I285
I284
IPS2_CS
neg. Logic
INT_PHI2_CPU {02}
I95
PHI2_CPU
INT_PHI2_SYS
I359
PHI2_SYS
INT_PHI2_VIA {02}
I146
PHI2_VIA
STATE_2 or State_6
INT_Q1 {02}
INT_Q0 {02}
I367
I358
RAM_RD
neg. Logic
INT_MAIN_CLOCK {02}
I365
I366
I205
RAM_WR
neg. Logic
INT_CPU_RW
RAM_WR is active in the last half of PHI2 because of memory protection in case of ABORT.
CPU_D0
I282
I267
INT_A16
CPU_D1
I281
I266
INT_A17
CPU_D2
I280
I265
INT_A18
CPU_D3
I279
I264
INT_A19
CPU_D4
I278
I260
INT_A20
CPU_D5
I277
I263
INT_A21
CPU_D6
I276
I262
INT_A22
CPU_D7
I275
I261
INT_A23
I299
PHI2_IN
I17
CPU_A15
I228
I351
INT_CPU_A15 {02}
CRT_RAM_FREE
I130
I350
INT_CRT_RAM_FREE {02}
INT_MAIN_CLOCK {02}
I353
neg. Logic
DMA_REQ
I131
I229
INT_DMA_REQ {02}
MAIN_CLOCK
I97
INT_MAIN_CLOCK {02}
neg. Logic
RESET
I96
I98
INT_RESET {02}
neg. Logic
ROM_ACCESS
I132
I134
INT_ROM_ACCESS {02}
CPU_RW
I207
INT_CPU_RW
MODE
I16
INT_MODE
0= Supervisory Mode
1= User Mode
INT_DMA_ACK
INT_A23
INT_A22
INT_A21
INT_A20
INT_A19
I271
I354
SEL_F8XX {02}
INT_A18
INT_A17
INT_A16
I161
Bank FF
I9
SEL_EXT {02}
I154
Bank FE
I8
SEL_ETH {02}
I153
Bank FD
I7
SEL_IDE {02}
I155
Bank FC
I5
SEL_CRT {02}
I152
Bank FB
I47
SEL_IPS2 {02}
I157
Bank FA
I55
SEL_VIA {02}
I289
Bank F9
I290
SEL_WDOG {02}
I311
Bank F8
I313
SEL_MMU {02}
INT_MODE
I18
0= Supervisory Mode
1= User Mode
I/O-Selection for FC0000 - FFFFFF
SEL_F8XX {02}
INT_A18
I302
INT_PHI2_SYS
I301
I303
SYS_OE
INT_CPU_RW
I300
I304
SYS_WR
CRT-RAM Select Logic
STATE_7 {02}
I335
I222
CRTBUF_ENABLE
neg. Logik
INT_CPU_RW
I334
I315
CRT_WRITE
neg. Logik
CNT4BUL
GND
GND
GND
GND
VCC
VCC
VCC
VCC
D0
D1
D2
D3
ENP
ENT
LD
CL
CK
Q0
Q1
Q2
Q3
CO
INT_MAIN_CLOCK {02}
I287
16/1 Divider
I288
KBD_SCAN_CLK
1,5 MHz Clock
INT_1_5_MHZ {02}
Lattice Semiconductor Corp.
5555 Northeast Moore Ct.
Hillsboro, Oregon 97124
Title: ASICCLK
Name: I/O-Section
Date: 27.01.2009
Sheet 1 of 2



Lattice Semiconductor Corp.	Title: ASICCLK	
5555 Northeast Moore Ct. Hillsboro, Oregon 97124	Name: Address Decoder	
	Date: 27.01.2009	Sheet 2 of 2